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TITLE: LOW RISE/FALL SKEWED INPUT BUFFER COMPENSATING  
PROCESS VARIATION  
INVENTOR(S): JONGHEE HAN

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The diagram shows a circuit with two main parts. The top part, labeled 401, is enclosed in a dashed box and contains two sub-circuits: a 'DIFFERENTIAL AMPLIFIER STAGE' (410) and an 'INVERTER STAGE' (420). The differential amplifier stage 410 has two inputs,  $V_{IN}$  and  $V_{REF}$ , and an 'ENABLE' input. It is connected to a common-mode feedback circuit (410) which includes a PMOS transistor and an NMOS transistor, both controlled by  $V_{IN}$ . The inverter stage 420 consists of a PMOS network (MP1, MP2) and an NMOS network (MN1, MN2). The output of the inverter stage is  $V_{OUT}$ . The bottom part of the diagram shows a current source circuit (410) with two PMOS transistors (MPC1, MPC2) and two NMOS transistors (MNC1, MNC2). The PMOS transistors are controlled by  $V_{R\_P}$  and  $V_{R\_N}$ , and the NMOS transistors are controlled by  $V_{IN}$ . The current source circuit is connected to the differential amplifier stage and the inverter stage.

FIG. 4

# REPLACEMENT SHEET

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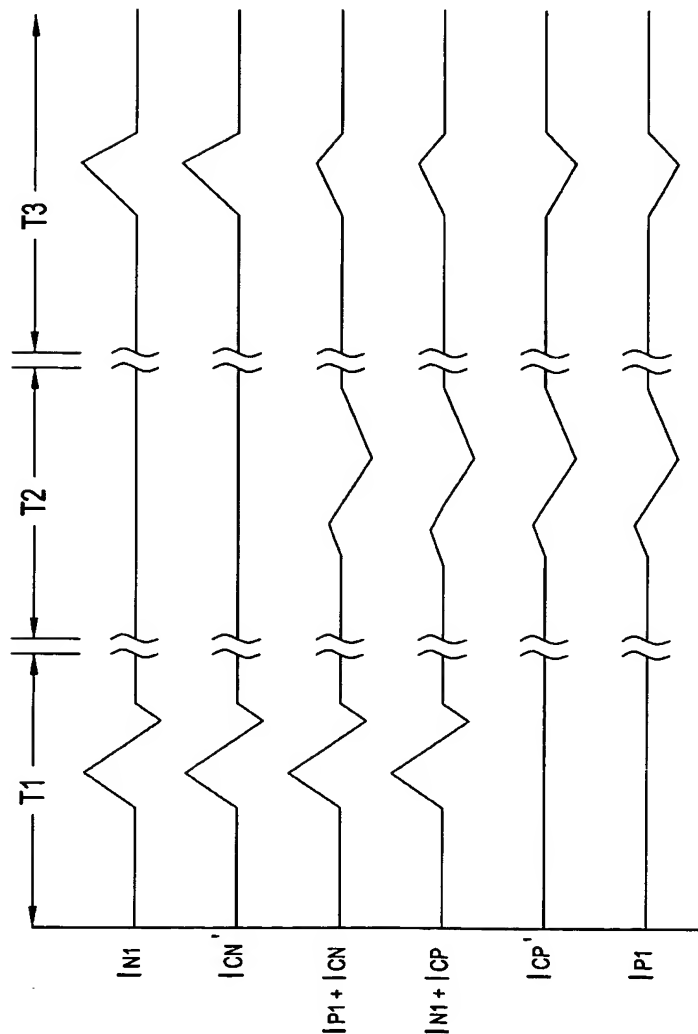


FIG. 5